CMOS Active Pixel Sensors for Low Power, Highly Miniaturized Imaging Systems

Multimedia, military, medical, and automotive applications will benefit from this second generation image sensor technology.

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The complementary metal-oxide-semiconductor (CMOS) active pixel sensor (APS) technology has been developed over the past three years by NASA at the Jet Propulsion Laboratory, and has reached a level of performance comparable to CCDs with greatly increased functionality but at a very reduced power level. The CMOS APS is poised to supplant CCDS in many applications, as well as open new markets and applications.

The CMOS APS uses microelectronics industry-standard CMOS technology to implement the image sensor. The continual reduction in microelectronics feature size permits the integration of both detector and readout amplifier within each pixel. The designed fill factor of APS pixels is typically 25-30% - comparable to interline transfer CCDS - and readily improved through the use of on-chip microlenses. Since each amplifier is only selected for readout, power dissipation is minimized. The standard 5 volt (or 3.3 volt) operation of the sensor also contributes to its minimal power dissipation (1 O -50 mW, depending on on-chip functionality and readout rate).

In 1993, JPL began the transfer of this technology to industry, and has technology collaboration agreements with several small companies as well as with Kodak, National Semiconductor, and AT&T. AT&T has already demonstrated a 1024xI 024 element APS with 10 micron pixel pitch,

The imaging performance of the sensors is quite good. Typical noise floors of 15 electrons r.m.s. are achieved, with the current record at JPL of 7 electrons r.m. s. at 100 kpix/sec. This is more than an order of magnitude improvement over previous CMOS image sensors or charge injection devices (250 e- r.m.s.), and competitive with nearly all CCDs. Conversion gain is typically 5-15 uV/e- with a saturation level of 1-1.5 volts (5 volt supply). This corresponds to a dynamic range of 75-80 dB, or 12-14 bits. On-chip circuits have been developed that reduce fixed pattern noise to less than 0.10/0 sat, and off-chip suppression is readily implemented for more demanding applications. Quantum efficiency, per pixel, is typically 30% since the readout area has some photosensitivity. Because there is no charge transfer in the APS, there is no smear. Anti-blooming protection is built into each pixel.

The CMOS technology used for APS implementation permits the easy integration of on-chip timing and control circuits, as well as analog signal chain electronics. JPL has built a 256x256 image sensor that essentially requires only 5 volts and a clock to produce high quality analog video output. Since the CMOS APS architecture is inherently random access, window of region readout is readily achieved, as is electronic pan and zoom.

Another important on-chip component now under research at JPL is the analog to digital converter (ADC). Such a chip has a full digital interface that simplifies system design. Several chips with 8-bit on-chip ADC have been demonstrated at JPL and AT&T. Improved resolution, higher speed, and lower power are desired,

Additional functionality has also been demonstrated in R&D sensors at JPL including multiresolution readout for robotics, very high frame rate imaging (simple to achieve in the APS compared to a CCD due to the in-pixel amplifier), and sensors with very high effective dynamic range (greater than 20 bits).

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